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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,093	12/29/2000	Michael Cornaby	2207/9806	6385

7590 01/18/2006

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,093	CORNABY ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States

3. Claims 18-26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Goss et al., US Patent 3,909,797.

4. Referring to claim 18 Goss et al. have taught a microinstruction sequencer, comprising:

a. a microinstruction sequencer stack comprising an array of memory cells (Figure 2, element 60, including elements 62, 64, 66, and 68); and

b. microinstruction sequencing logic associated with the microinstruction sequencer stack (Figure 2), wherein the microinstruction sequencing logic is responsive to an operation code that includes a first field for non-microinstruction sequencer stack operations (column 5, lines 50-55, sequential, non-branch opcodes in the instruction format) and a second field for microinstruction sequencer stack operations (column 2, lines 50-67, branch field),

5. Referring to claim 19, Goss et al. have taught a microprocessor including a microinstruction sequencer comprising:

a. an array of memory cells dedicated to a microinstruction sequencer stack (Figure 2, elements 62, 64, 66, and 68);

b. an address multiplexer coupled to the array of memory cells (Figure 2, element 54);

c. sequencing logic coupled to the address multiplexer and to the array of memory cells (Figure 2), wherein the sequencing logic is responsive to an operation code that includes a first field for non-microinstruction sequencer stack operations (column 5, lines 50-55, sequential, non-branch opcodes in the instruction format) and a second field for microinstruction sequencer stack operations(column 2, lines 50-67, branch field); and

d. a microprocessor core unit coupled to the array of memory cells (The entire system in Figure 1 is a microprocessor core unit.).

6. Referring to claim 20, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction includes instructions to:

a. generate a value of a microinstruction address (Figure 2, Element 56 contains the generated microinstruction address.);

b. add an intermediary value to the value of the microinstruction address to yield an incremented value (Figure 2, element 58);

c. send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.); and

e. push the incremented value onto the microinstruction sequencer stack (Abstract, Column 7, lines 60-64).

7. Referring to claim 21, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to:

i. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

ii. send the popped value to a microinstruction address multiplexer (Figure 2, element 54).

8. Referring to claim 22, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction includes instructions to:

a. send a control value to the microinstruction sequencer stack, said control value to:

b. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

c. send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52), said immediate logic to pass the value to a microprocessor core unit (Figure 2, Element 52 passes the value to the core unit.).

9. Referring to claim 23, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction includes instructions to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to push a value in an

immediate field of a microinstruction onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.).

10. Referring to claim 24, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction includes instructions to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to return to a reset state (Inherent, Must be able to initialize the system to a known state.).

11. Referring to claim 25, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 send control values to the stack.), said control value to cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62) and send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52).

12. Referring to claim 26, Goss et al. have taught the microinstruction sequencer of claim 18, as described above, and wherein the microinstruction includes instructions to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic (abstract, column 8, lines 49-62, Figure 2, elements 54, 56, 50, and 52).

13. Referring to claim 27, Goss et al. have taught the microinstruction sequencer of claim 19, as described above, and wherein the microprocessor core unit is an execution unit (Figure 1).

14. Referring to claim 28, Goss et al. have taught the microinstruction sequencer of claim 19, as described above, and wherein the microprocessor core unit is a retire unit (Abstract, column 2, lines 39-44, In order for the instructions in the subroutine to be completed, there must inherently be unit that performs the completing.).

Response to Arguments

15. Applicant's arguments with respect to claims 18-26 have been considered but are moot in view of the newly applied ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

1/6/06

HENRY W. H. TSAI
PRIMARY EXAMINER